REMARKS

Claims 1-12 are pending in the application, claims 7-12 have been withdrawn. Claim 1 has been amended. Support for the amendment to claim 1 is supported by the originally filed specification, e.g., Figs 3 to 6 and corresponding description. No new matter has been added. Applicants respectfully request reconsideration of these claims.

In paragraph 1 on page 2 of the Office Action, the Examiner objects to claim 4. Applicant submits herewith amended claim 4 to assist in overcoming the objection.

Applicant respectfully requests the Examiner withdraw the objection to claim 4.

In paragraph 3 on page 2 of the Office Action, claims 1-10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Tang (US 6,211,092) in view of Watatani (US 6,153,511). Applicants respectfully traverse the rejection.

The present invention comprises a method for, *inter alia*, fabricating an integrated circuit having at least one metallization plane is claimed in the present invention wherein in a plurality of several steps metal-containing contacts and lines of a further metallization plane are produced for providing an electric contact between the at least one metallization plane and the further metallization plane through the contact holes. The present invention is based on the problem to quickly and easily produce metal-containing contacts and lines in metallization planes and to avoid contaminants throughout said production.

For producing the metal-containing contacts and lines according to the present invention, firstly, contact holes and line trenches are formed in a four layer stack situated on the at least one metallization plane and, secondly, said contact holes and line

trenches are filled with metal. The formation of the contact holes and line trenches is based on different etching processes using masks and having a special order.

According to the present invention, at least the following steps of the claimed method are used for the formation of the contact holes and line trenches:

1. A first structured mask having openings corresponding to the arrangement of the contact holes is placed above the four layer stack.
2. A first non-selective etching process is applied to the four layer stack at regions being uncovered by the first structured mask, i.e. a partial etching of the four layer stack takes place. The ending of said first non-selective etching process depends on the relation of the thicknesses of the second and fourth dielectric layers. If the second dielectric layer (which is situated below the fourth dielectric layer) is thinner than the fourth dielectric layer, holes are non-selectively etched at the places of said contact holes only into said fourth dielectric layer until the distance between the bottom of said hole and the top of the third dielectric layer (which is situated between the second and the fourth dielectric layers) is essentially equal to the thickness of said second dielectric layer. However, if the second dielectric layer is thicker than the fourth dielectric layer, holes are non-selectively etched at the places of said contact holes into said second dielectric layer through said fourth dielectric layer as well as the third dielectric layer until the distance between the bottom of said hole and the top of the first dielectric layer (which is situated below the second dielectric layer) is essentially equal to the thickness of said fourth dielectric layer. This second step can be described as an adjusting step, which adjusts the thickness of the material in the hole which still has to be removed to

expose the first layer and the thickness of the material in the trench line which still has to be removed to expose the third layer to an amount that is essentially the same.

3. Then, the first structured mask is removed from the four layer stack.
4. A second structured mask having openings corresponding to the arrangement of the line trenches is placed above the four layer stack wherein said holes formed in the above mentioned 2nd step remain uncovered.
5. A second non-selective etching process is applied to the four layer stack at regions being uncovered by the second structured mask. Now, the line trenches are non-selectively etched into said fourth dielectric layer while said second non-selective etching process also ensures that said holes formed in the above mentioned 2nd step obtain a larger depth and extend into said second dielectric layer. The increasing depth of said holes gradually corresponds to the increasing depth of the line trenches. This means, the second part of the formation of said contact holes takes place in passing during the formation of said line trenches. Said second non-selective etching process ends shortly before uncovering said first and third dielectric layers in said holes and line trenches, respectively.
6. Afterwards, the second and fourth dielectric layers are etched selectively with respect to the first and third dielectric layers in regions where the contact holes and the line trenches shall be formed until the underlying surfaces of the first and third dielectric layers are uncovered in each case.

7. Finally, the first and third dielectric layers are etched in regions where the contact holes and the line trenches shall be formed until the underlying surface is uncovered in each case.

According to the present invention, the etching processes mentioned above in the steps 2 and 5 are non-selective which means that the main material removal takes place in short time since non-selective etching has high etching rates. Further, the selective etching processes mentioned above in the steps 6 and 7 need only short time due to the little remaining dielectric material which has to be removed.

None of the documents cited in the above mentioned Office Action teaches alone or in combination with each other to form the contact holes and line trenches as in present claim 1.

Tang (US 6 211 092 B1) discloses in Fig.3 to Fig.7 as well as in the corresponding description parts the following processing method:

1) using a four layer stack (12, 14, 16, 20) of four dielectric layers;
2) applying a first structured mask (44) having a first opening (46) corresponding to the arrangement of a contact hole (50') above the four layer stack (12, 14, 16, 20);
3) timed non-selectively etching the second, third and fourth dielectric layers (14, 16, 20) below the first opening (46) of the first structured mask (44) to form a hole (50);
4) selectively etching the second dielectric layer until the surface of the first dielectric layer (12) is uncovered. Thus, the hole (50) is formed by only using the first structured masks;
5) removing the first structured mask (44);

6) applying a second structured mask (56) having a second opening (58) corresponding to the arrangement of a line trench (62) above the four layer stack (12, 14, 16, 20) and aligned to the hole (50);

7) selectively etching the fourth dielectric layer (20) below the second opening (58) of the second structured mask (56) to form the line trench (62) until the surface of the third dielectric layer (16) is uncovered, thereby forming a contact hole (50') from the hole (50); and

8) selectively etching the first and third dielectric layers (12, 16) at the bottom of the contact hole (50') and of the line trench (62) until underlying surface is uncovered.

Therefore, it is disclosed in *Tang* to form the hole, from which the contact hole results, during a non-selective/selective etching process using only a first etching mask. After the complete formation of the hole, i.e. the uncovering of the first dielectric layer, the line trench is formed during an etching using a second etching mask and exclusively using a selective etching process.

As mentioned by the examiner *Tang* does not teach etching into the fourth and the second dielectric layer using the second etching mask. Further, it has to be mentioned that according to the present invention this etching into the fourth and the second dielectric layer using the second etching mask is partially carried out using a non-selective etching process. Furthermore, it has to be mentioned that *Tang* does not teach a step corresponding to the above mentioned second step of the method of the present invention. Furthermore, according to the claims of the present invention the etching using the first etching mask is only carried out using non-selective etching, while according to *Tang* is carried out at least partially using selective etching.

Watatani (US 6 153 511 A) discloses in Fig.5A to Fig.5G and the corresponding description parts the following processing method:

A) using a six layer stack (72, 74, 76, 78, 80, 82) of six dielectric layers;

B) applying a first structured mask (84) having a first opening (84A) corresponding to the arrangement of a line trench (91) above the six layer stack (72, 74, 76, 78, 80, 82);

C) selectively etching the sixth dielectric layer (82) below the first opening (84A) of the first structured mask (84) to form a hole (82A) until the surface of the fifth dielectric layer (80) is uncovered;

D) removing the first structured mask (84);

E) applying a second structured mask (86) having a second opening (86A) corresponding to the arrangement of a contact hole (89) above the six layer stack (72, 74, 76, 78, 80, 82) and aligned to the hole (82A);

F) selectively etching the fifth dielectric layer (80) below the second opening (86A) of the second structured mask (86) until the surface of the fourth dielectric layer (78) is uncovered;

G) selectively etching the fourth dielectric layer (78) below the second opening (86A) of the second structured mask (86) until the surface of the third dielectric layer (76) is uncovered;

H) removing the second structured mask (86);

I) selectively etching the third and fifth dielectric layers (76, 80) below the hole (82A) formed in the sixth dielectric layer (82) until the surfaces of the second and fourth

dielectric layers (74, 78) are uncovered, wherein the sixth dielectric layer (82) functions as a hard mask;

J) selectively etching the second and fourth dielectric layers (74, 78) below the hole (82A) formed in the sixth dielectric layer (82) until the surfaces of the first and third dielectric layers (72, 76) are uncovered, wherein the third, fifth and sixth dielectric layers (76, 80, 82) function as hard masks; and

K) selectively etching the first and third dielectric layers (72, 76) below the hole (82A) formed in the sixth dielectric layer (82) until the underlying surface of the first dielectric layer (72) is uncovered, wherein the second, fourth, fifth and sixth dielectric layers (74, 78, 80, 82) function as hard masks.

Therefore, it is disclosed in *Watatani* to form the contact hole (89) and the line trench (91) only during selective etching processes. Thus, the formation of contact holes and of line trenches by means of the method disclosed in *Watatani* needs much more time than the method disclosed in *Tang* because only selective etching processes with low etching rates are used.

Thus, the problem of the present invention to easily decrease the production time of metal-containing contacts and lines in metallization planes can even not solved by the method disclosed in *Watatani*. Therefore, a person skilled in the art dealing with the above mentioned problem of the present invention would even not use the disclosure and teaching of *Watatani* for solving that problem.

Even if a person skilled in the art would combine the teaching of *Tang* and the teaching of *Watatani* he would not come to the process according to claimed invention. If he combines the teaching of *Tang* and the teaching of *Watatani* to use a second mask

for forming the hole and the trench line he would come to the conclusion that he has to use selective etching for the etching with the second mask. This is the case since firstly *Tang* as well as *Watatani* only disclose to use selective etching with the second mask, i.e. as soon as etching for forming the trench line is involved only selective etching is disclosed, and secondly the person skilled in the art knows, since the thickness of the material which has to be removed to uncover the third layer in regions where the trench line is formed and the thickness of the material which has to be removed to uncover the first layer in regions where the contact hole is formed is different, only selective etching can be used to ensure that this etching step does not etches the first and/or the third layer.

The use of a non-selective etching step together with the second etching mask is possible only in combination with the claimed "adjusting step". For this adjusting step the person skilled in the art neither gets a hint from the teaching of *Tang* nor from the teaching of *Watatani*.

Thus, even the combination of the disclosures of *Tang* and *Watatani* would not solve the above mentioned problem to be solved by the present invention since none of both teaches or gives any hint how to easily decrease the production time of metal-containing contacts and lines in metallization planes.

The partial usage of non-selective etching processes while using the second etching mask instead of selective etching processes as described in the present invention has the great advantage that due to the higher etching rate the non-selective etching processes are much quicker and, thus, that the present invention has a higher process throughput yielding in clearly reduced processing costs.

Three criteria must be met to establish a *prima facie* case of obviousness. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference. Second, there must be a reasonable expectation of success. Finally, the prior art reference, or combination of references, must teach or suggest all the claim limitations. MPEP § 2142.

Therefore, claim 1, as amended, is not obvious over Tang in view of Watatani as the combination fails to disclose all of the claims limitations recited in claim 1.

Applicants respectfully request withdrawal of the rejection of claim 1 under 35 U.S.C. §103 as being obvious over Tang in view of Watatani.

Dependent claims 2-10, which are dependent from independent claim 1 were rejected under 35 U.S.C. §103(a) as being unpatentable over Tang in view of Watatani. While Applicants do not acquiesce with the particular rejections to these dependent claims, it is believed that these rejections are moot in view of the remarks made in connection with amended independent claim 1. These dependent claims include all of the limitations of the base claim and any intervening claims, and recite additional features which further distinguish these claims from the cited references. Therefore, dependent claims 2-10 are also in condition for allowance.

Applicants respectfully request withdrawal of the rejection of claims 2-10 under 35 U.S.C. § 103(a) as being anticipated by Tang in view of Watatani.

In view of the amendments and reasons provided above, it is believed that all pending claims are in condition for allowance. Applicants respectfully request favorable reconsideration and early allowance of all pending claims.

If a telephone conference would be helpful in resolving any issues concerning this communication, please contact Applicants' attorney of record, Jeffrey R. Stone at (952) 253-4130.

Respectfully submitted,

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